PROCESS DEVELOPMENT FOR HETEROJUNCTION IBC CELLS ON THIN SILICON FOILS BONDED TO GLASS

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ABSTRACT: We describe the process for fabricating interdigitated back-contacted cells compatible with thin (40µm) monocrystalline silicon foils. Throughout the process, the foils are supported by either the silicon parent substrate, or by a host (glass) superstrate using adhesive bonding. For a number of process steps, we describe possible issues, boundary conditions and performance. Using the integrated process which is fully compatible with bonded foils, cells were fabricated on a freestanding, non-textured wafer. An efficiency of 18.0% was achieved, the main limitations being the absence of surface texturing and a non-optimized amorphous silicon emitter.
Keywords: a-Si:H, Amorphous Silicon, Back Contact, Encapsulation, Heterojunction, Porous Silicon, Si-Films

1 INTRODUCTION

In order to reduce the material cost for silicon solar cells, several research groups are investigating the feasibility of making cells on very thin monocrystalline silicon foils [1][2][3]. Imec proposed the so-called i²module approach (integrated interconnect-module), which allows for the module-level processing of interdigitated back-contacted cells (IBC) on foils that are bonded to a glass superstrate [4]. The fabrication process obviously has to be compatible with the specific device structure and materials, in particular glass and bonding agent. This restricts the number of available options for process development. In this contribution we review the current status of the process development and the limitations in cell performance.

2 OVERVIEW OF DEVICE PROCESSING

Starting from the fabrication of the silicon foil, we will introduce the device processing step-by-step. Figure 1 shows a schematic cross-section of the targeted device, a crystalline silicon / a-Si:H heterojunction IBC cell. The reasons for this choice of material will become clear from the discussion.

2.1 Epitaxial foil

The targeted process for the fabrication of foils has been extensively described elsewhere [5]. In short, highly p^+ doped Czochralski substrates are anodically etched to produce porous silicon. After baking at 1130°C in H_2 environment, the porous layer is re-organized and produces a smooth, 1—2µm thick layer which is only weakly bonded to the parent substrate (Figure 2). The layer serves as a template for subsequent epitaxial silicon deposition (40µm). After detachment from the parent substrate through cleavage at the high porosity layer this results in the desired epitaxial foil.

While this process has been shown to produce high quality material [6], we are not yet able to porosify substrates in large quantities. For the development and fabrication of solar cells on foils we therefore temporarily resort to foils where the porous layer has been obtained by means of DUV lithography and dry etching. The remaining process steps (H_2 bake and epitaxial deposition) are almost identical and result in 40µm thick foils of high crystalline quality.

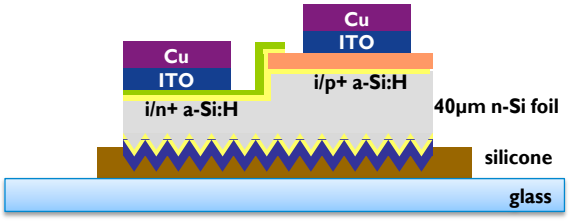

Figure 1: Schematic cross-section of the heterojunction IBC cell on bonded silicon foils.

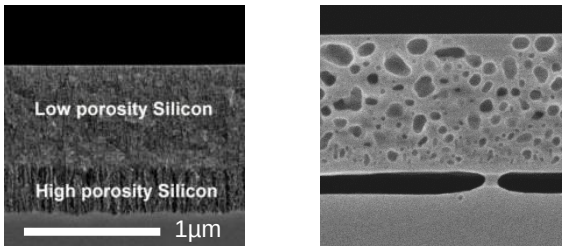

Figure 2: Formation of thin silicon foils using porous silicon etching (left-hand image) followed by high temperature anneal in hydrogen (right-hand image). The resulting restructured porous-Si layer serves as a template for subsequent epitaxial deposition.

2.2 Front surface texturing

For efficient light coupling, obviously the front surface of the cell needs to be textured. Conventionally this is done by means of alkaline etching, resulting in random pyramid formation. However, the amount of silicon that is removed in this step (a layer of 3-5µm thickness) can be quite

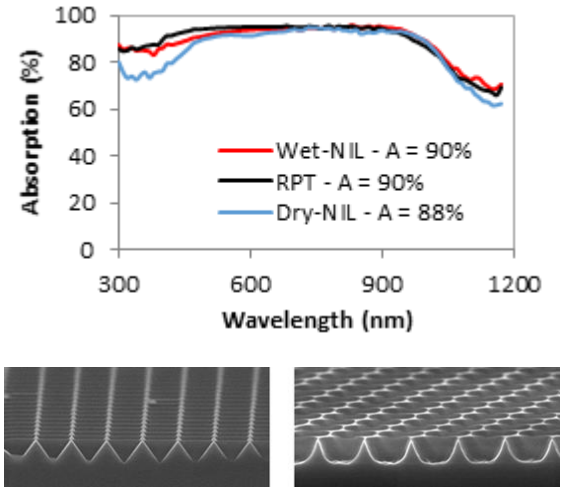

Figure 3: Optical absorption as measured on IBC cells on 40µm silicon foils. Curves are shown for random pyramid texturing and NIL based texturing. The wet-etched and dry-etched NIL textures are shown in the tilted SEM photographs below (the pattern has a period of 800nm).

significant compared to the foil thickness. For this reason we are investigating alternative texturing methods, based on Nano Imprint Lithography (NIL). In this approach, a resist layer on the foil frontside is patterned using a polymer stamp. The pattern is then transferred to the foil by means of dry or alkaline wet etching, which removes only a few 100 nm.

We have found that wet etching allows for better surface passivation, whereas dry etching induces damage to the surface [7][8]. For the current stamp design, the optical performance is overall similar to that of random pyramid texturing (Figure 3), NIL being more effective in light trapping but with a lower anti-reflective performance.

2.3 Front passivation, antireflective coating

One critical aspect in the process before foil detachment is the requirement that the process should not induce damage to the foil, neither should it affect the detachment process itself. We have found [5] that when the thermal budget exceeds 800°C for extended times, it is no longer possible to reliably detach the foils from the parent. As a result, front surface field formation by means of $POCl_3$ diffusion is not recommended. Similarly, high quality surface passivation by means of thermal oxidation is not possible.

There are several alternatives available for low temperature surface passivation. In view of the low optical absorption, atomic layer deposition of metal oxides is an interesting option. We have currently chosen to passivate the front surface by PECVD of hydrogenated amorphous silicon a-Si:H.

The choice for a-Si:H as surface passivation layer implies the requirement of a low temperature antireflective coating. PECVD of silicon nitride can be done at temperatures as low as 200°C without affecting the a-Si:H surface passivation. Indeed, the positive charges in the SiN_x layer induce an additional beneficial surface field effect. Using a combination of 8 nm intrinsic a-Si:H and low-temperature SiN_x, we have achieved J_0<4fA/cm^2 on pyramid textured n-type CZ substrates.

2.4 Bonding

After processing of the front surface, the size of the foils is defined by laser dicing (typically 110mm × 110mm, with rounded corners). The glass superstrates (156mm × 156mm), to which the foils should be bonded, are cleaned and a bonding agent is applied in an area of approximately 115mm × 115mm, larger than the foil area. The foils are detached and bonded to the glass in vacuum, which results in a high quality bond without any bubble formation. An additional outgassing step is applied through vacuum curing at 200°C.

The choice of the bonding agent is critical. Different two-part silicones were evaluated for their bonding properties. Typically we observed a trade-off between tackiness (adhesion force) and a spontaneous wetting of the rear side of the substrate by the uncured silicone. In view of the later processing to be done, this spontaneous wetting is undesirable. The issue has been resolved by applying a optimized pre-curing step before bonding.

2.5 Rear side passivation

After bonding, the rear side of the cell is exposed, as well as the glass superstrate and some silicone along the edge of the cell. The rear side process should be compatible with these exposed materials. For example, the presence of the silicone imposes a temperature budget of 200°C to the rear side process. For this reason, we choose a-Si:H for the formation of the emitter and the back surface field (BSF).

It is well known that the presence of exposed silicone can have a dramatic impact on the quality of a-Si:H passivation [9]. This impact depends strongly on the processing conditions and on the type of silicone that is used [10]. We have found that it is possible to modify the exposed silicone such that it exhibits an improved compatibility with the a-Si:H deposition process [11]. The modification is achieved by an Ar or O_2 plasma treatment, followed by a mild wet cleaning of the silicon surface. After this silicone treatment, we achieve good passivation by depositing a-Si:H (i/p$^+$), resulting in J_0<10fA/cm^2 as measured on bonded n-type CZ substrates.

2.5 Patterning process

Several approaches to patterning of HJ-IBC emitter, BSF and contacts have been reported, including deposition through a shadow mask [12], lift-off [13] and lithography [14]. Although it is understood that neither of these options is ideal, we are currently using a lithographic process on bonded foils. Over time, this will be replaced by a "litho-free" process which is more appropriate for large scale, module-level processing.

Etching of the a-Si:H (i/p$^+$) emitter can be achieved with a dilute $BHF/HNO_3/H_2O$ solution which shows good compatibility with the photoresist etch mask. One problem with this etching step is the inhomogeneous etch rate of the aSi:H (p$^+$), which results in excessive surface roughness (Figure 5) resulting in a less effective passivation by a-Si:H (i/n$^+$) (Figure 6). For this reason, we are currently investigating possible alternatives such as dilute Buffered $HF/H_2O_2/H_2O$ mixtures and dry etching.

The etchant which is needed to etch a-Si:H (i/p$^+$) is not selective, which means that the underlying Si substrate is etched as well. In contrast, etching of the a-Si:H (i/n$^+$) BSF is done with a 1% TMAH solution at room temperature. This etchant is selective against the emitter layer, and

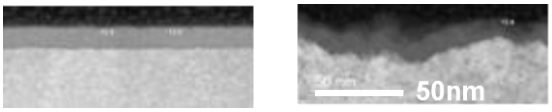

Figure 5: TEM pictures of the substrate surface before (left) and after (right) etching a-Si:H (i/p$^+$) with dilute BHF/HNO_3/H_2O.

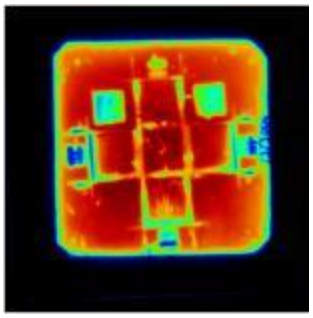

Figure 6: Photoluminescence (PL) image of a bonded n-type FZ substrate after emitter patterning and re-passivation with a-Si:H (i/n+). The areas with lower PL intensity correspond to regions where a-Si:H (i/p+) was etched away, resulting in high surface roughness and less effective passivation.

therefore stops once the a-Si:H (i/p$^+$) layer is reached [15]. This is the reason why the a-Si:H (i/n$^+$) layer is deposited after patterning of the emitter, and not vice versa.

The removal of photoresist is a critical process since, like the silicone, its presence can have a severe impact on the subsequent deposition of a-Si:H layers (in the current case, the BSF). The stripping sequence that was found to be both effective and compatible with the exposed silicone is a sequence of acetone, isopropyl alcohol and a SC1 mixture at 50°C (NH_4OH/H_2O_2/H_2O, 1/1/5). Care should be taken since this latter solution etches a-Si:H (p$^+$) at a rate of 0.1 nm/min. After patterning of the a-Si:H (i/n$^+$) BSF, the SC1 solution is preferably not used since the etch rate is even higher at 0.3 nm/min.

2.6 Metallization

For the rear side contact we use a stack of indium-tin-oxide (ITO, with an optimized work function) and Cu. This combination exhibits good rear side reflectance, which is of particular importance for thin cells. The sputter damage which is induced during the ITO deposition can be repaired by a 5 min. anneal at 150°C. Using this stack on two-sided test structures with a-Si:H (i/n$^+$) and (i/p$^+$), we have been able to achieve V_{oc} values in excess of 710 mV.

3 DEVICE RESULTS

The process that was described above is fully compatible with substrates that are bonded to glass with silicone. So far, however, it has only been applied to freestanding wafers to demonstrate the quality of the individual process steps. The cells were fabricated on an n-type FZ wafer (thickness 200µm, resistivity 3 Ω-cm) and had an area of 2cm × 2cm. It should be stressed that we present here the results on a wafer which was not textured. The results are shown in Table 1.

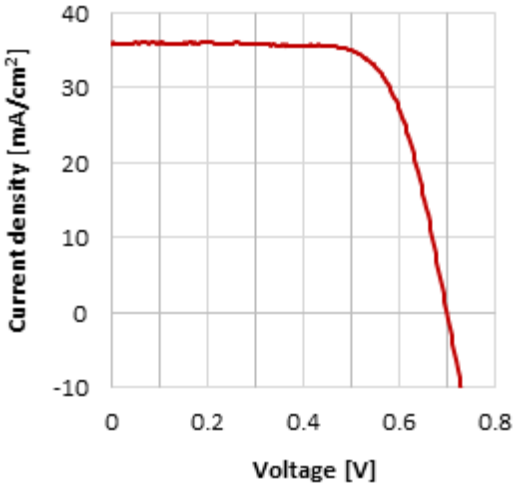

Figure 4: Light J-V curve of the best HIT-IBC cell, achieved on a non-textured 200µm n-type FZ wafer. Cell area is 3.96 cm^2.

Table 1: Cell results as obtained using the fabrication process described in the text.

	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	η [%]
average of 5	35.5	693	70.4	17.3
best of 5	**35.8**	**701**	**72.0**	**18.0**

The short circuit current J_{sc} compares well with a calculated value of 35.8 mA/cm^2 which one may expect based on the measured optical dispersions of a-Si:H. Using the simulation tool OPAL [14], the current loss due to reflection can be estimated to be 5.5 mA/cm^2, whereas the absorption in the a-Si:H is of the order of 3 mA/cm^2. We expect to improve J_{sc} by texturing (approximately 3.5 mA/cm^2) and by reduction of the a-Si:H layer thickness, or by using an alternative low-temperature passivation method such as atomic layer deposition of Al_2O_3.

The V_{oc} value is significantly lower than expected based on the passivation tests described above. The most likely cause of this is the increase in surface roughness during a-Si:H (i/p$^+$) patterning. Alternative techniques to etch this layer are expected to increase the quality of the surface passivation substantially.

The Fill Factor (FF) is quite low in these cells, and is mainly attributed to the high series resistance of approximately 2 Ω-cm^2 caused by the a-Si:H (i/p$^+$) stack. Recent investigations indicate that this resistance can be significantly reduced by optimization of the deposition process.

4 SUMMARY

We have described the current status in process development for heterojunction IBC devices compatible with thin (40µm) silicon foils. Functional cells on 200µm n-type FZ substrates have been fabricated, and issues limiting the device performance have been identified. On-going process development is expected to improve the cell efficiency significantly. After stabilisation of the process flow, device processing will be implemented on epifoils.

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